**CMSC 411 Homework Assignment 1 Due Date: Sep 21, 2022**

**1.** Describe Moore’s Law in your own words.

**2.** How does a machine understand the code you write?

**3.** Consider three different processors P1 and P2 executing the same instruction set. P1 has a 3 GHz clock rate and a CPI of 2. P2 has a 2 GHz clock rate and a CPI of 1.0.

1. Which processor has the highest performance expressed in instructions per second?
2. If the processors each execute a program in 20 seconds, find the number of cycles and the number of instructions.
3. We are trying to reduce the execution time by 20% but this leads to an increase of 30% in the CPI. What clock rate should we have to get this time reduction?

**4.** Assume that for a program, compiler A results in a dynamic instruction count of 1.0E9 and has an execution time of 1.2 s, while compiler B results in a dynamic instruction count of 1.2E9 and an execution time of 1.6 s.

1. Find the average CPI for each program given that the processor has a clock cycle time of 1 ns.
2. Assume the compiled programs run on two different processors. If the execution times on the two processors are the same, how much faster is the clock of the processor running compiler A's code versus the clock of the processor running compiler B's code?
3. A new compiler is developed that uses only 6.0E8 instructions and has an average CPI of 1.1. What is the speedup of using this new compiler versus using compiler A or B on the original processor?

**5.** Convert 2DA.57 from hexadecimal to octal.

**6.** Find out the 2’s complement of 10110001.

**7.** Suppose for machine A, for 10 clock cycles and 2ns clock cycle time. If the CPU time is the same for machine B as machine A, Calculate the clock cycle time for 20 clock cycles for machine B.

**8.** The Pentium 4 Prescott processor, released in 2004, had a clock rate of 4 GHz and voltage of 1.5 V. Assume that, on average, it consumed 11 W of static power and 92 W of dynamic power.

The Core i5 Ivy Bridge, released in 2012, had a clock rate of 3.5 GHz and voltage of 1.2 V. Assume that, on average, it consumed 32 W of static power and 45 W of dynamic power.

1. For each processor find the average capacitive loads.
2. Find the percentage of the total dissipated power composed by static power and the ratio of static power to dynamic power for each technology.

**9.** Two different compilers are being tested for a 500 MHz machine with three different classes of instructions: Class A, Class B, and Class C, which require 1, 2, and 3 cycles (respectively).

Both compilers are used to produce code for a large piece of software.

The first compiler's code uses 6 million Class A instructions, 2 million Class B instructions, and 2 million Class C instructions.

The second compiler's code uses 7 million Class A instructions, 1 million Class B instructions, and 2 million Class C instructions.

1. Which program uses fewer instructions?
2. Which sequence uses fewer clock cycles?
3. Find out CPI for both compilers.